FPGA Based DAQ System for RPC Based Particle Detector

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Talk Outline

- About the INO ICAL Experiment
- ICAL Detector and Construction
- What is expected from the DAQ in ICAL
- The Overall DAQ Scheme
- RPC-DAQ Module
The INO ICAL Experiment

- ICAL is Iron-Calorimeter to be set up by the India-based Neutrino Observatory (INO) collaboration, inside an underground cavern, to study neutrinos.
- The ICAL will study atmospheric neutrinos to determine their mass hierarchy among other things.
- The ICAL will use magnetized iron as its target mass and glass Resistive Plate Chambers as the active detector element.
Neutrinos

- Neutrinos are charge less leptons along with the charged leptons the electrons, muons and taus.
- Neutrinos are extremely elusive, i.e. they are extremely less interactive because of negligible mass and no charge.
- Because of extremely less probability of interaction with matter, neutrino detectors need to be very massive.
- They come in 3 flavours:
  - electron neutrinos ($\nu_e$), muon neutrinos ($\nu_\mu$), and tau neutrinos ($\nu_\tau$)
ICAL Detector and Construction

RPCs sandwiched between Iron plates: 150 layers

No of Modules: 3
No. of Layers: 150
No. of RPCs per Layer: 64
No. of RPC units: 28,800
No. of readout strips: 3,686,400

An RPC Model showing orthogonal pick-up strips
Muon Tracks in the ICAL

ZZ:YY:XX \{TrackType== -1 \&\& (ENum==16)\}
What is expected from the DAQ in ICAL

- Identify physics events in the detector by forming a trigger
- Track the muons formed from the neutrino interaction with Iron by storing the detector state during an event
- Find directionality of neutrinos through tracking and timing
- Monitor RPC health
  - RPC noise rate
  - RPC chamber Current
  - Pulse profiling
- Carry out Calibrations
  - Pulse Amplitudes
  - TDC (Time to Digital Convertor) Offsets
- Slow Control and Monitoring
  - High Voltage
  - Low Voltage
  - Ambient parameters, temperature, pressure and RH
Overall ICAL DAQ Scheme

1. A Few Servers
2. DAQ Servers
3. 1 set per RPC
4. 28,800 RPCs
5. Front-End (Amplifiers and Discriminators)
6. 1 STM per 160 RPCs
7. Tier-1 Network Switch
8. 1 per Tier-1 Switch
9. From Other Tier-1 Switches
10. Segment Trigger Modules
11. From Other STMs
12. 1 ST M
13. Global Trigger Module
14. Global Signal Fan-out
15. To Other RPCs
16. 1 per RPC
17. Tier-1 Network Switch
18. From Other Tier-1 Switches
19. Network Interface
20. Waveform Sampler
21. Ambient Monitor
22. Rate Scalars
23. To Other RPCs
24. Multi-hit TDC
25. Strip Hit Latch
26. Pulse Shapers
27. Soft-core Controller
28. Ambient Monitor
29. 11th Sep 2015
30. Mandar Saraf, TIFR
31. IEEE Bombay Section Symposium
32. FPGA based RPC-DAQ Module
33. Front-End (Amplifiers and Discriminators)
34. RPCs
RPC-DAQ Module
Input/Output to the Module

- Unshaped digitized RPC signals from 128 strips (64x + 64y), in LVDS form
- (16 analog RPC signals for pulse profiling.)
- Global trigger input – from the Trigger Subsystem
- Global clock for synchronising time stamping on each board
- TDC calibration signals
- TCP-IP connection to backend for command and data transfer
- SPI interface for High Voltage Module Control and Monitoring
- Pre-Trigger outputs
Functions of the Module

- The RPC-DAQ board is required to collect following information from the incoming RPC pulses.
  - Asynchronous event data on each trigger:
    - Strip hit data: event pattern across the 128 strips.: Track reconstruction
    - Timing data: relative arrival times of muons at different layers (belonging to the same event).: To get muon directionality
    - RPC pulse widths and profiles
  - Periodic data:
    - Strip rates: Noise rate observed for each strip. (RPC and electronics’ health).
    - Ambient parameters: Temperature, relative Humidity and Pressure.
    - RPC Current from the local HV DC-DC (RPC Health).
    - RPC High Voltage, from the local HV DC-DC.
- Generate Trigger Primitives (1/2/3/4 Fold) for final trigger formation
Design Considerations/Constraints

- Data rates
- Physical dimensions: Owing to huge constraints on the space availability the RPC-DAQ board has very limited size.
- Service life of the electronics is expected to be 15 years, so component spares availability is a concern.
- Component Selection considering
  - Long service life
  - Power consumption
  - Cost
RPC-DAQ Features

- 128 LVDS inputs to cater for 64x and 64y strips of a 2m x 2m RPC
- Ethernet connectivity for data and command interface to the back-end server
- Facility for remote firmware upgradation
- Ambient parameters monitoring, viz., Temperature, Humidity and Pressure
- NIOS Processor working at 100MHz, sustained trigger rate of 4kHz
FPGA

- It is the heart of the RPC-DAq Module
- The FPGA will accept LVDS signals from the preamps and process them
- It will house all the logic required for daq, in addition to housing the on board microprocessor
- We require an FPGA with 400+ user I/Os including 140 LVDS pairs
- Presently we are testing our systems on Altera Cyclone IV FPGAs
- Looking at Xilinx **Spartan 6 LX100** and **Altera Cyclone IV CE115 FPGA**
N/W Interface for RPC-DAQ

- The ICAL electronics will use a TCP/IP based network interface to send and receive data from front-end to the back-end.
- Every RPC will become a network node.
- Wiznet W5300 is used to provide a network interface.
- W5300 supports hardwired TCP/IP protocols.
Microprocessor

- The processor acts as a simple process controller and helps in communicating with the backend
- Data from various sources on the RPC-DAQ is packed and sent to the backend via N/W
- Carries out RPC-DAQ system settings as asked by backend
- It assists in FPGA remote configuration (firmware upgradation)
- A soft core processor, configured into the FPGA, like NIOS-II from Altera can be used very effectively.
Microprocessor System

- OnChip RAM 400kB
- RTC
- RPC-DAQ Logic
- RPC-DAQ Logic Bridge
- W5300_INT
- EVE_INT
- MON_INT
- Interrupt Logic
- FPGA
- NIOS CORE
- W5300 Bridge
- HPTDC Bridge
- EPCS Flash Controller
- SPI Bridge
- JTAG Debug
- JTAG Port
- W5300
- HPTDC
- EPCS FLASH
- TPH Sensor System
TDC

- Timing information will be required to find the directionality of Muons
- This can be inferred from the relative arrival times of pulses across the vertical direction of ICAL
- Hence the need of a TDC
- Using HPTDCs developed by the CERN collaboration
The RPC-DAQ Board

125 mm
Data Size and Rate

- Event Data per Trigger is as follows: (64 strips on each plane of RPC)
  - Strip hit data = 128 bits
  - TDC data = 1 channel for 8 strips and two edges per hit, up to 4 hits per channel per event = 16 channels x 2 edges x 4 hits x 32 bits = 4096 bits
  - RPC ID = 32 bits
  - Event Number = 32 bits
  - Time Stamp = 64 bits
  - Pulse Profile Data = 16 channels x 50nS x 4GSPS x16 bits = 51200 bits
  - Header = 32 bits
  - Data size per event per RPC
  - \( D_R = 128 + 4096 + 32 + 32 + 64 + 51200 + 32 = 55,584 \text{ bits} \)
  - For 10Hz trigger rate, Max. Data Rate at each RPC = 54.28 kbps
Data Size and Rate continued…

- Monitoring Data per 10 seconds
  - We require to monitor at least 8 pick-up strips per plane of RPC at a time.
  - Monitor Data per strip + Channel ID = 24 + 8 = 32 bits
  - RPC ID = 32 bits (RPC ID == RPC Network IP Address)
  - Mon Event Number = 32 bits
  - Ambient Sensors’ data = 3 x 16 bits = 48 bits
  - Time Stamp = 64 bits
  - Pulse Profile data = 1000 pulses (if noise rate is 100Hz) x 16 bits x 100 samples = 1,600,000 bits
  - Header = 32 bits
  - Data size per 10 seconds per RPC
    \[ D_R = 24 + 8 + 32 + 32 + 48 + 64 + 2048 + 1600000 + 32 = 1,602,288 \text{ bits} = 1564.7 \text{ kbits} \]
  - **Max Data Rate with 10 second monitoring period per RPC**
    \[ = 156.47 \text{ kbps} \]
Timing Stats of Event Data Processing by Front End Processor

Event FIFO length = 2048 32bit words
Wiznet event socket Tx Memory = 18KB

Time taken (Closing & Opening Gate) with
Worst Case data (16 Channel TDC) (600 bytes) = 110us

Only reading event data from H/W & writing into event FIFO

Best case (1 Channel TDC) (120 bytes) = 16us
Worst Case data (16 Channel TDC) (600 bytes) = 100us

Reading from event FIFO & writing to wiznet FIFO 600 bytes = 165us

Time taken by wiznet to PUSH data into network from wiznet FIFO (Checking for Send ok)
600 bytes = 60us

Throughput with random TDC size and periodic triggers = 3.5KHz
**Event Data Processing Scheme Test with Measurement of event loss percentage at various rates (1 KHz to 10 kHz Random triggers) with Fixed & variable Event size**

<table>
<thead>
<tr>
<th>Random Triggers Mean Freq (KHz)</th>
<th>Event Triggers Sent (millions)</th>
<th>10 TDC Channels 408 bytes</th>
<th>5 TDC Channels 248 bytes</th>
<th>1 TDC Channels 120 Bytes</th>
<th>Random TDC Data size</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>Events Rcvd</td>
<td>Loss (%)</td>
<td>Events Rcvd</td>
<td>Loss (%)</td>
</tr>
<tr>
<td>5</td>
<td>3</td>
<td>2983965</td>
<td>0.6</td>
<td>2999955</td>
<td>0.001</td>
</tr>
<tr>
<td>10.1</td>
<td>3</td>
<td>1551048</td>
<td>48.3</td>
<td>2570990</td>
<td>14.4</td>
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</table>

<table>
<thead>
<tr>
<th>Random Triggers Mean Freq (KHz)</th>
<th>Event Triggers Sent (millions)</th>
<th>16 TDC 600 bytes -52</th>
<th>Random TDC Data size (8 - 548)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>Events Rcvd</td>
<td>Loss (%)</td>
</tr>
<tr>
<td>5</td>
<td>3</td>
<td>2268343</td>
<td>24.6</td>
</tr>
<tr>
<td>10.1</td>
<td>3</td>
<td>1147293</td>
<td>62.8</td>
</tr>
</tbody>
</table>
Current Status

- 5 RPC-DAQs have been built and lab tested
- They have now been interfaced to detectors in the INO lab at TIFR, for testing field performance
Thank You

On behalf of the Electronics Team, INO Collaboration
Physics driven detector requirements

- Should have large target mass (50-100 kT)
- **Good tracking and energy resolution** (tracking calorimeter)
- **Good directionality, up/down discrimination** (< 1 nSec time resolution)
- Nearly $4\pi$ coverage in solid angle (except near horizontal)
- Good charge identification capability (magnetic field 1.5 Tesla)
- Modularity and ease of construction (3 modules of ~17 kTons each)
- Compliment capabilities of existing and proposed detectors
Future Upgrades

- Addition of Digital Pulse Sampler
- Addition of on board threshold generation circuitry for the Front-End Amplifier
- Upgrade of Ambient Sensors, some of them are obsolete now
ICAL Data Size & BandWidth Requirement

- BW at RPC = 54.28 + 156.47 = 210.75 kbps
- BW at Layer = 210.75 x 64 RPCs = 13.17 Mbps
- BW at Module = 13.17 x 150 Layers = 1.92 Gbps
- Total BW for 3 Modules = 5.79 Gbps

- Hourly Data Size
  - Data Size = 5.79 Gbps x 3600 / 8 = 2.54 TBytes
Wiznet W5300 Interface

- Altera Cyclone II FPGA on DE2 Kit
- NIOS II System
  - NIOS II Core
  - JTAG UART
  - System Interconnect Fabric
  - Generic Tristate Controller
  - OnChip Memory
- Wiznet WIZ830MJ
  - Wiznet W5300
  - Ethernet PHY
  - RJ45 with Magnetics
  - To N/W Switch

- Add(9..0)
- Data(15..0)
- nWR
- nRD
- nCS
W5300 Performance

• While using Wiznet in TCP mode Data Transmission is reliable as every byte sent is received correctly at the destination.

• Majority of time is spent in “writing to FIFO”. Aim should be to reduce this time to increase the data rate.

• We are able to achieve 18 Mbps data rate (for single socket) by increasing the NIOS2 clock frequency up to 100MHz. If we can reduce the FIFO write time up to 50ns/byte (minimum time as per datasheet of W5300) then the throughput rate estimation is coming near to 50 Mbps.

• Also we observed that the optimal packet size for data transfer is 1280 bytes.
Power Usage

- Power estimate for major components
  - FPGA: Roughly 1.5W
  - HPTDC: In low resolution low power mode, 40MHz clock and with TTL inputs: 0.45W
  - Wiznet W5300: Auto-negotiation of internal PHY: 0.825W
  - DRS4: @ 6GSPS: 0.35W
- Total estimated power is less than 5W (3.125W), i.e. less than 2A @ 3.3V
- If we have a bus voltage of 5V, then regulators drop 1.7V and waste less than 4W of power
- Thus total power dissipated is less than 10W
Power Supply

- All components studied so far require only a single supply voltage
  - In fact this has to be design constraint, considering integration issues
- If the maximum voltage required by any component is 3.3V, then we can run a 5V bus around the system, and use onboard regulators to derive required voltages
Back End Ethernet Switches

- Proposal is for uplinking the FE Switches to back end switches to which the computers are also connected.
- BE Switches: Commercial 48 port gigabit switches (copper/fiber) with at least 4 10G uplink ports
- Rack size is 1U (all current models)
- Many models have MAC address table exceeding 10k, so can store location information of all RPC's of one ICAL module. Implications are (to be tested):
  - the Master computer can quickly address any RPC
  - no need of L3 functionality, L2 functionality will do
  - but time taken to gather the MAC table.. to be understood
- IP segmentation using separate class C subnet for each 3 layers
Functional Tests Carried Out

- Power supply circuit checked
- Event Latch Test from every input
- HPTDC test for various delays (Input to Trigger) from a few inputs, and fixed delays from all inputs.
- Pre-Trigger signal generation checked
- Wiznet network interface for UDP and TCP checked
- Flash memory programming using Altera’s Serial Flash Loader tool
A View of the ICAL
The RPCs

- Operate in Avalanche mode
- 64 pickup strips each in X and Y planes
- Pulse Amplitude 5-10mv
- Pulse width ~20ns
- Pulse Rise Time <1ns
### ICAL Factsheet

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>No. of modules</td>
<td>3</td>
</tr>
<tr>
<td>Module dimensions</td>
<td>$16\text{m} \times 16\text{m} \times 14.5\text{m}$</td>
</tr>
<tr>
<td>Detector dimensions</td>
<td>$48.4\text{m} \times 16\text{m} \times 14.5\text{m}$</td>
</tr>
<tr>
<td>No. of layers</td>
<td>150</td>
</tr>
<tr>
<td>Iron plate thickness</td>
<td>56mm</td>
</tr>
<tr>
<td>Gap for RPC trays</td>
<td>40mm</td>
</tr>
<tr>
<td>Magnetic field</td>
<td>1.3Tesla</td>
</tr>
<tr>
<td>RPC dimensions</td>
<td>$1,950\text{mm} \times 1,840\text{mm} \times 24\text{mm}$</td>
</tr>
<tr>
<td>Readout strip pitch</td>
<td>30mm</td>
</tr>
<tr>
<td>No. of RPCs/Road/Layer</td>
<td>8</td>
</tr>
<tr>
<td>No. of Roads/Layer/Module</td>
<td>8</td>
</tr>
<tr>
<td>No. of RPC units/Layer</td>
<td>192</td>
</tr>
<tr>
<td><strong>No. of RPC units</strong></td>
<td>$28,800 (97,505\text{m}^2)$</td>
</tr>
<tr>
<td><strong>No. of readout strips</strong></td>
<td>$3,686,400$</td>
</tr>
</tbody>
</table>
Back End Systems

- Configuration or Control of RPC DAQ via Ethernet
- Trigger Logic
  - Event trigger: Segmented or Global Trigger on a Physics event
    - Trigger initiates data recording in RPC DAQ
- Data transfer to Central node over Ethernet
  - Event Data transfer
  - Monitor Data Transfer
- Collating distributed data
  - Event time stamp
  - TDC synchronization
- PC Clusters
  - Data Concentrator and Event Builder
  - Data Management
  - Pre-analysis and Monitoring
- Slow Control Monitoring
  - LV & HV
  - Gas system
N/W Switches on the face of Spacers

Tier-1 N/W Switch
40mm x 80 x 200mm
RPC-DAQ Module